Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **RESET**
2. **CLK**
3. **N. CLK**
4. **VBB**
5. **VEE**
6. **N. Q**
7. **Q**
8. **VCC**

**KL32**

**AC76**

**MASK**

**REF**

**2**

**3**

**1 8**

**4 5**

**7**

**6**

**.041”**

**.041”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size = .0033 x .0033”**

**Backside Potential:**

**Mask Ref: KL32 / AC76**

**APPROVED BY: DK DIE SIZE .041” X .041” DATE: 4/23/19**

**MFG: ON SEMI THICKNESS .008” P/N: MC100EL32**

**DG 10.1.2**

#### Rev B, 7/1